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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/866,319	05/25/2001	Jeffrey B. Johnson	BUR920010011US1	5556

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EXAMINER

FARAHANI, DANA

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 07/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/866,319

Applicant(s)

JOHNSON ET AL.

Examiner

Dana Farahani

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 28 May 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-44 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-44 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-19 and 21-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jalali-Farahani et al., hereinafter Jalali (U.S. 5,620,907) in view of Streetman (Solid State Electronic Devices), all previously cited.

Regarding claims 1-3, 12, 24-27, 34, 35, and 36, Jalali discloses, a method of fabricating a semiconductor device comprising the steps of providing a collector 20 and a subcollector 10; forming a base 60; and an emitter 80; all of figure 1. Furthermore, Jalali discloses a typical range of thickness for the collector region is 1000-10000 Angstrom.

Jalali does not disclose the layer over the subcollector is a diffusion layer, or width and doping concentration of the diffusion layer.

It is well known in the art that diffused layers are used extensively in IC fabrication, and appropriate width and doping concentration of the collector layer are part of every transistor design (see Streetman, page 144, first paragraph under the title diffusion). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use this commonly used method to make a collector

Art Unit: 2814

layer over the subcollector layer Jalali discloses since this method is widely available, and to control the breakdown voltage and the base widening, respectively.

Regarding claims 4, 5, 28, and 29, Jalali discloses in column 2, lines 55-60 and column 3, lines 35-40 that the doping concentration of the upper part of the collector layer has a lower doping level; compare to both the subcollector layer and the base layer.

Regarding claims 6, 7, 30, and 31, Streetman discloses B, P, As, and Sb are used in diffusion. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made since these materials have the highest rate of the diffused atoms as a function of temperature in Si solid solubilities (see Appendix VII).

Regarding claims 8, 22, and 23, Jalali does not disclose ion implantation and Annealing to form a diffusion layer (or a subcollector layer). However, it is well known in the art that ion implantation and Annealing are used in the art because of low temperature needed and the thermal budget advantage, respectively (see page 149, the second paragraph; and page 147, the second paragraph). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use these alternatives because of the thermal budget advantage.

Regarding claims 13 and 32, Jalali discloses collector layer 50 is formed between the other collector layers and the base 60. Jalali dose not disclose this layer is lightly doped. It would have been obvious to one of ordinary skill in the art at the time the invention was made to lightly dope this layer in order to reduce the resistance of it (see column 2, lines 60-62).

Regarding claims 15, 39, and 40, see Jalali, column 4, lines 10-20.

Regarding claims 16 and 41, Jalali discloses in figure 1, the base region 60 is SiGe, while layers 40, 70, and 90 are polysilicon and layer 80 is single crystal.

Regarding claims 17 and 42, there is a patterned insulator layer 100 on the SiGe layer with an opening, as shown in Jalali, figure 1, and forming polysilicon layer 110 in the opening (see column 5, lines 1-9).

Regarding claim 18, see Jalali, column 6, lines 11-19.

Regarding claims 19 and 43, see Jalali, column 2, lines 63-67.

Regarding claim 21, although Jalali does not disclose CVD is being used for depositing SiGe layer. It is well known in the art that this process is commonly used as deposition method for layers (see Streetman, page 151, the second paragraph). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use this method to deposit the SiGe layer since it is widely available, and to control breakdown voltage and widening of the .

Regarding claims 9, 10, 11, 14, 33, 37, and 38, Jalali discloses the claimed invention except for the values the applicant has disclosed. it would have been obvious to one of ordinary skill in the art at the time the invention was made to include these values, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art.

3. Claims 20 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jalali as applied to claim 16 above, and further in view of King et al., hereinafter King (U.S. 6,087,683).

Art Unit: 2814

Jalali discloses the claimed invention except the SiGeC layer. King discloses that this material is used in heterojunction devices because of its low band gap (see column 4, line 13; and column 3, lines 55-65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention to use this material in the heterostructure bipolar transistor Jalali disclose because of its low band gap.

### ***Response to Arguments***

4. Applicant's arguments filed on 5/28/02 have been fully considered but they are not persuasive.

Applicant's argument that none of the references state or suggest that "...a subcollector and a diffusion, wherein the diffusion has a vertical width sufficiently narrow to avoid lowering the collector-base breakdown voltage and a doping sufficiently high to restrict base widening when the base-emitter junction is forward biased" is not found persuasive.

These features (appropriate collector doping and appropriate collector vertical width) are so well known in the art that they are practically part of every bipolar junction transistor process design (see Prior Art below).

### ***Prior Art***

The prior art is made of record and not relied upon is considered pertinent to applicant's disclosure, See for example Semiconductor Devices, Physics and Technology by S.M. SZE, page 77, formulas 14b-17a; and page 103, formula 86.

***Conclusion***

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (703)305-1914. The examiner can normally be reached on M-F 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703)306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Application/Control Number: 09/866,319  
Art Unit: 2814

Page 7

Dana Farahani  
July 12, 2002



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